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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
TON, MY TRANG	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 10/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/808,122	CHIH ET AL.	
	Examiner	Art Unit	
	My-Trang N. Ton	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-13 and 15-21* is/are rejected.

7)☒ Claim(s) *7,14 and 22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 July 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

MY-TRANG NU TON
PRIMARY EXAMINER

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

Claims 3-6 and 15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 3, the limitation "a first NMOS transistor directly coupled to the high operating voltage ... " is misdescriptive of the present invention since such limitation is not seen as recited therein. In order to avoid any confusion, Applicant is required to particularly point out how this limitation reads on the circuit arrangement of the drawings. As seen in Figs. 2a, 3a, a first NMOS transistor (i.e, 208) is coupled to the high operating voltage (Vpp via transistors 206 and 204).

Claim 5 is similarly rejected as claim 3: the limitation "a first PMOS transistor directly coupled to the low voltage ..." is misdescriptive of the present invention since such limitation is not seen as recited therein. In order to avoid any confusion, Applicant is required to particularly point out how this limitation reads on the circuit arrangement of the drawings. As seen in figs. 2a, 3a, a first PMOS transistor (i.e. 206) is coupled to the low voltage (Ground via transistors 208 and 210).

Claims 4 and 6 are rendered indefinite by the deficiencies of claims 3 and 5.

Claim 15 recites the limitation "the input signal" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-6, 8, 10, 12-13, 15-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Lall et al (U.S Patent No. 6,370,071) cited in PTOL 1449.

***** *After further consideration, the rejection for claims 12-13, 15-17 are now included. It appears that these claims were inadvertently overlooked. It is now believed these claims are similarly rejected as below claims.*

Lall et al discloses in Fig. 4 a high voltage CMOS switch circuit including:

Regarding claim 1: one (P2) or more transistors (P2, P4) of a same type connected in series and being operable with a normal operating voltage (EN) and a high operating voltage (Vpp);

a high operating voltage (Vpp) coupled to a first end of the device (first end coupled to P2) of the device structure (300);

a low voltage (Ground) coupled to a second end (coupled to N2); and

one (hvb) or more control voltages controllably coupled to the gates of the transistors (hvb coupled to gate of P2);

wherein at least one of the control voltages (hvb) coupled to the gate of at least one transistor (P2) is raised to a medium voltage level (Vpp – resistive loss from P1,P3) that is substantially higher than a normal operating voltage (VEN) and lower than the high operating voltage (Vpp) when operating under the high operating voltage (Vpp) for

tolerating stress imposed thereon by the high operating voltage (due to P1, P3 have resistance values, the voltage at hvb = Vpp minus the resistive loss from resistive path P1, P3, thus, hvb will be substantially lower than Vpp).

Regarding claim 2: the medium voltage level is about one half of the high operating voltage (hvb = Vpp – the resistive loss from P1,P3 is about one half of the high operating voltage Vpp (when Vpp =3.3V)).

Regarding claim 3: Due to indefiniteness, the limitation "a first NMOS transistor directly coupled to the high operating voltage" does not given sufficient weight to read over the prior art. Element N4 reads on a first NMOS transistor coupled to the high voltage (Vpp via P2, P4) and element N2 reads on at least one second NMOS transistor serially coupled between the first NMOS transistor (N4) and the low voltage (Ground), the control voltage being coupled to a gate of the first NMOS transistor (N4).

Regarding claim 4: the low voltage is a ground voltage (Ground)

Claim 5 is similarly rejected as claim 3: Due to indefiniteness, the limitation "a first PMOS transistor directly coupled to the low operating voltage" does not given sufficient weight to read over the prior art. Element P4 reads on a first PMOS transistor, and element P2 reads on at least one second PMOS transistor.

Regarding claim 6: the transistor have separated N wells (see P2, P4).

Regarding claim 8: the high operating voltage is above 10V (Vpp is pumped up to 13 volts, see col. 5, line 2-5).

Regarding claim 10: the stress is a gated stress (P2, P4).

Claim 12 is similarly rejected as claim 1:

a first cascade device structure (P2, P4) having one or more P type transistors (P2, P4) connected in series with one end thereof connected to the high operating voltage (Vpp);

a second cascade device structure (N2, N4) in series with the first cascade device structure (P2, P4) at its other end having one or more N type transistors (N2, N4); and

one ore more control voltages (hvb) controllably coupled to the gates of the transistors (P2) in the first and second cascade device structure for raising voltages on one or more gates of the transistors to one or more medium values that are above the normal operating voltage for tolerating voltage stress imposed by the high operating voltage (the voltage at hvb = Vpp – the resistive loss from resistive path P1, P3: that is above the normal operating voltage VEN for tolerating voltage stress imposed by the high operating voltage Vpp).

Regarding claim 13: element EN reads on an input module.

Regarding claim 15: the control voltages for the first and second cascade device structures are controlled separately depending on the input signal (hvb controlled P2, Vcc controlled N4).

Regarding claim 16: the second cascade device structure is further connected to a grounding voltage (N4, N2 are connected to Ground).

Regarding claim 17: the transistors in the first cascade device structure have separate N wells (see P2, P4).

Regarding claim 18:

a first cascade device structure (P2, P4) having one (P2) or more (P2, P4) P type transistors connected in series with one end thereof connected to the high operating voltage (P2 connected to Vpp); and

one (hvb) or more control voltages controllably coupled to the gates of the transistors (hvb coupled to gate of P2) in the first cascade device structure (P2) for raising voltages on one (P2) or more gates of the transistors to one or more medium values (hvb = Vpp – resistive loss from P1,P3) that are substantially above the normal operating voltage (EN) and below the high operating voltage (Vpp) for tolerating voltage stress imposed by the high operating voltage (the voltage at hvb = Vpp – the resistive loss from resistive path P1, P3 that is higher than VEN, and less than Vpp due to resistive loss);

wherein the P type transistors have separated N wells (see P2, P4 and col. 2, lines 52-54, and col. 5, line 66 – col. 6, line 3).

Regarding claim 19: a second cascade device structure (N4, N2) in series with the first cascade device structure (P2, P4) at its other end having one or more N type transistors (N4, N2).

Regarding claim 20: the control voltages (hvb, Vcc, ENB) for the first and second cascade device structure (P2, P4, N4, N2) are controlled separately depending on the input signal (EN).

Regarding claim 21: the second cascade device structure (N4, N2) is further connected to a grounding voltage (Ground).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 9 and 11 remain rejected under 35 U.S.C. 103(a) as being unpatentable over Lall et al as applied to claims 1 and 8 above.

As stated above, every element of the claimed invention recited in above claims can be seen in the circuit of Lall. However, this reference does not specially show "the normal operating voltage is below 2V" as recited in claim 9 and "the stress is a gated stress" as recited in claim 11.

Although Lall et al do not expressly state the value for the normal operating voltage, this difference is not of patentable merit because it is notoriously well known in the art that different values for the operating voltage can be selected in order to produce correspondingly different output values. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize the normal operating voltage EN is below 2 volts in realizing the circuit of the Lall et al reference for the purpose of producing different output values when different values of the operating voltage is selected.

Regarding the limitation "the stress is a drain stress" recited in claim 11: this appears to be obvious variations (i.e.., not patentably distinct) to limitations "the stress is a gated stress". Therefore, it would have been obvious to one of ordinary skill in the art

to employ (the stress is a drain stress for P2, P4), as they appear to be obvious variations (not patentably distinct) and yielding same functional device.

Allowable Subject Matter

Claims 7, 14 and 22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art disclosed or suggested to show the particular structure and/or the particular operation recited in these claims namely: "the control voltages are determined so that the stress imposed by the high voltage is about equally divided by the transistors in the device structure" (claim 7); "an input module ... raised to a predetermined medium value" (claims 14 and 22).

Response to Arguments

Applicant's arguments filed 7/25/05 have been fully considered but they are not persuasive. Examiner has thoroughly reviewed Applicant's arguments but firmly believes that the cited reference reasonably and properly meet the claimed limitation as rejected.

Applicant's argument – "the signal hvb is not substantially lower than the high operating voltage Vpp".

Examiner's response - because P1 and P2 of Lall have resistance values, thus, the voltage at hvb will not be equal to the high operating voltage Vpp. The voltage at hvb will be equal to Vpp minus the resistive loss from the resistive path P1, P3, thus, the limitation "substantially ... lower than the high operating voltage" is clearly met as

recited in claims 1 and 18. Therefore, these claims are not seen to distinguish the present invention over the Lall's reference.

Regarding col. 6, lines 29-33: although Lall discloses the signal hvb is at Vpp when EN is Low. However, one ordinary skill in the art as routine design expedients know that due to the resistive loss from the resistive path P1, P3, the voltage at hvb will be less than the high operating voltage Vpp.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to My-Trang N. Ton whose telephone number is 571-272-1754. The examiner can normally be reached on 7:00 a.m - 5:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

My-Trang N. Ton
Primary Examiner
Art Unit 2816

October 11, 2005